



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,756	01/14/2004	Hajime Kimura	12732-207001 / US6910	1526
26171 7590 08/09/2007 FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER PIZIALI, JEFFREY J	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 08/09/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/756,756

Applicant(s)

KIMURA ET AL.

Examiner

Jeff Piziali

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-18, 27-66, 70-78 and 80-84 is/are pending in the application.
- 4a) Of the above claim(s) 1-10, 13-18, 27-66, 70-78 and 80 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11, 12 and 81-84 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 October 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 5/24/07 & 8/10/06.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Drawings***

2. The drawings were received on 27 October 2005. These drawings are acceptable.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 11, 12, and 81 are rejected under 35 U.S.C. 102(b) as being anticipated by *Koyama et al (US 2001/0048408 A1)*.

Regarding claim 11, Koyama discloses a signal line driver circuit [Fig. 1] comprising: a shift register [Fig. 1; First - Third Shift Registers]; a latch circuit [Fig. 1; LAT Portion], electrically connected to the shift register, comprising a plurality of pairs of current sources [Fig. 5B], each of which is configured to receive a set signal [Fig. 5B; Control Signals 1 & 2] and a signal current [Fig. 5B; Input], and to control an output current value [Fig. 5B; Output] corresponding to the signal current (see Pages 5-6; Paragraphs 88-89); and a changing over

Art Unit: 2629

circuit [Fig. 1; 10a] electrically connected to the plurality of pairs of current sources and a plurality of signal lines [Fig. 1; S001 - S640], wherein the changing over circuit selects one pair of current sources from the plurality of pairs of current sources for electrically connecting to each of the plurality of signal lines, and wherein the set signal is an output of the shift register (see Page 3; Paragraphs 50-53).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 11; furthermore, Koyama discloses a signal line driver circuit [Fig. 6] comprising: a shift register [Fig. 6; First - Third Shift Registers]; a latch circuit [Fig. 1; Latch Circuit Portion], electrically connected to the shift register, comprising: a plurality of pairs of current sources [Fig. 5B], each of which is configured to receive a set signal [Fig. 5B; Control Signals 1 & 2] and a signal current [Fig. 5B; Input], and to control an output current value [Fig. 5B; Output] corresponding to the signal current (see Pages 5-6; Paragraphs 88-89); a first switch (see Fig. 5B) provided between the shift register and each of the plurality of pairs of current sources (see Pages 5-6; Paragraphs 88-89); and a second switch [Fig. 6; 20] (see Page 6; Paragraphs 90-92), and a changing over circuit [Fig. 6; 10c] electrically connected between the plurality of pairs of current sources through the second switch and a plurality of signal lines, wherein the changing over circuit selects one pair of current sources from the plurality of pairs of current sources for electrically connecting to each of the plurality of signal lines, wherein the set signal is an output of the shift register, and wherein the first and second switches are controlled by a latch pulse [Fig. 1; LP] (see Page 3; Paragraphs 50-53).

Regarding claim 81, this claim is rejected by the reasoning applied in rejecting claims 11 and 12; furthermore, Koyama discloses a signal line driver circuit [Fig. 1] comprising: a plurality of current source circuits [Fig. 5B], each of which is supplied a first current [Fig. 5B; Input] and supplies a second current [Fig. 5B; Output] corresponding to the first current (see Pages 5-6; Paragraphs 88-89); a plurality of signal lines [Fig. 1; S001 - S640]; and a selector circuit [Fig. 1; 10a] electrically connected between the plurality of current source circuits and the plurality of signal lines, the selector circuit selecting one of the plurality of signal lines to which the second current is supplied (see Page 3; Paragraphs 50-53).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Art Unit: 2629

7. Claims 82-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Koyama et al* (US 2001/0048408 A1) in view of *Akimoto et al* (US 6,850,216 B2).

Regarding claim 82, Koyama discloses each of the current sources [Fig. 5B; transistor pairs] includes at least one transistor having a gate, and controlling a voltage [Fig. 5B; Control Signals 1 & 2] applied to the gate of the transistor (see Page 3; Paragraphs 50-53). One having ordinary skill in the art would recognize Koyama's gate controlling voltages [Fig. 5B; Control Signals 1 & 2] would necessarily and inherently be set via at least one switch -- otherwise the control signals would remain constant and provide no "control" whatsoever over Koyama's SRAM circuit.

However, should the applicants prove the Koyama reference neglects to teach such switch control with sufficient specificity; Akimoto does disclose current sources including at least one switch [Fig. 27; 201 & 202] and at least one transistor [Fig. 27; 205 & 206] having a gate, with the switch being connected to control a voltage applied to the gate of the transistor (see Column 1, Lines 10-53).

Koyama and Akimoto are analogous art, because they are from the shared inventive field of controlling SRAM type circuitry. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use Akimoto's switches to set Koyama's controlling voltages [Koyama: Fig. 5B; Control Signals 1 & 2], because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 83, this claim is rejected by the reasoning applied in rejecting claim 82.

Regarding claim 84, this claim is rejected by the reasoning applied in rejecting claim 82.

### ***Response to Arguments***

8. Applicants' arguments filed 24 May 2007 have been fully considered but they are not persuasive.

The applicants contend, the cited prior art of *Koyama et al (US 2001/0048408 A1)*, "*does not describe or suggest a current source configured to receive a set signal and a signal current, and to control an output current value corresponding to the signal current*" (see Page 19 of the 'Amendment in Reply to Action of January 22, 2007' filed 24 May 2007). However, the examiner respectfully disagrees.

Koyama discloses a current source circuit [Fig. 5B; transistor pair], which is configured to receive a set signal [Fig. 5B; Control Signals 1 & 2] and a signal current [Fig. 5B; Input], and to control an output current value [Fig. 5B; Output] corresponding to the signal current [Fig. 5B; Input] (see Pages 5-6; Paragraphs 88-89).

The applicants argue, "*the storage circuit of Fig. 5B of Koyama, which the rejection equates with the recited current source, comprises an SRAM circuit that does not control an output current corresponding to an input signal current and, instead, sets an output potential based on an input potential*" (see Page 19 of the 'Amendment in Reply to Action of January 22, 2007' filed 24 May 2007). However, again the examiner respectfully disagrees.

Ohm's law states that the electrical current passing through a conductor between two points is proportional to the potential difference (i.e. voltage drop or voltage) across the two points, and inversely proportional to the resistance between them (i.e.,  $I = V/R$ ). Clearly, resistance is held constant across Koyama's SRAM circuit in Figure 5B. The applicants themselves concede Koyama's "output potential [is] based on an input potential." Therefore, Koyama's input/output current will inherently be proportional to the input/output voltage. As such, Koyama's SRAM circuit would indeed control an output current [Fig. 5B; Output] corresponding to an input signal current [Fig. 5B; Input], as instantly claimed. Perhaps the simplest example of such an input-to-output current signal correspondence is that absent an input current signal, no output current signal will exist in Koyama's SRAM circuit. However, once an input current signal is applied to Koyama's current source circuit [Fig. 5B; transistor pair], and control signals 1 and 2 are switched turn the corresponding transistors on, a current signal will be output.

Applicants' arguments with respect to newly added claims 82-84 have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.



***Conclusion***

9. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2629

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Jeff Piziali  
6 August 2007